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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CANNING, ANTHONY J	
ART UNIT	PAPER NUMBER
2879	

DATE MAILED: 01/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,914	ITO ET AL.	
	Examiner	Art Unit	
	Anthony J. Canning	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-14 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement of Amendment

1. The amendment to the instant application was entered on 27 October 2005.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al. (U.S. 5,315,206).

4. As to claim 9, Yoshida et al. disclose a method of manufacturing an electron source device, including: subjecting a metal substrate to electrolytic oxidation, thereby forming an oxide substrate having a number of small through holes, each of which opens to both surfaces of the metal substrate (see Fig. 5, items 12 and 17; column 5, lines 30-33, lines 52-68); column 6, lines 15-26); burying an electron-emitting material in the through holes of the oxide substrate (see Fig. 4, item 20; column 5, lines 52-53); forming a first electrode on one surface of the oxide substrate, the first electrode contacting the electron-emitting material (see Fig. 4, item 21; column 6, lines 3-7); and forming a second electrode on another surface of the oxide substrate (see Fig. 4, item 23; column 6, lines 3-7), the second electrode insulated from the electron-emitting material (see Fig. 4, item 11; column 5, lines 22-28).

5. As to claim 10, Yoshida et al. disclose the method of manufacturing an electron source device, according to claim 9, wherein an electrolysis voltage is controlled, in the electrolytic oxidation, to control the diameter of the small through holes (column 6, lines 15-41).

6. As to claim 11, Yoshida et al. disclose the method of manufacturing an electron source device, according to claim 9, wherein an electrolysis time is controlled, in the electrolytic oxidation, to control the diameter of the small through holes (column 13, lines 27-34).

7. As to claim 19, Yoshida et al. disclose a method of manufacturing an electron source device of a flat display app

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 12, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida et al. (U.S. 5,315,206) in view of Jin et al. (U.S. 5,648,699).

10. As to claim 12, Yoshida et al. disclose the method of manufacturing an electron source device, according to claim 9. Yoshida et al. fail to disclose that the electron-emitting material is buried in the through holes by introducing an organic substance into the through; and then baking the organic substance to carbonize the substance.

Jin et al. disclose that the electron-emitting material is buried in the through holes (see Fig 9, item 147; column 4, lines 58-67; column 5, lines 1-7; column 8, lines 30-36) by introducing an organic substance into the through holes (column 5, lines 8-15); and then baking the organic substance to carbonize the substance (column 5, lines 8-9; the examiner interprets heating the coating as baking). Jin et al. further disclose that introduction of an organic substance improves adhesion of the emitter particles (column 5, lines 11-13).

Therefore, it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the method of manufacturing an electron source of Yoshida et al. to include an organic substance introduced into the through-holes, as taught by Jin et al., for the added benefit of improved adhesion of the emitter particles.

11. As to claim 14, Yoshida et al. disclose the method of manufacturing an electron source device, according to claim 9. Jin et al. further disclose that the electron-emitting material is buried in the through holes by vapor-depositing an organic substance in the through holes (column 5, lines 7-15; the application of the organic substance is through spray[1] coating). Jin et

[1] a jet of vapor or finely divided liquid

al. further disclose that the organic substance improves adhesion of the emitter particles (column 5, lines 11-13).

Therefore, it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the method of manufacturing an electron source of Yoshida et al. to include an organic substance introduced into the through-holes, as taught by Jin et al., for the added benefit of improved adhesion of the emitter particles.

12. As to claim 19, Yoshida et al. disclose a method for manufacturing an electron source device of a flat display apparatus (column 1, lines 14-17; flat CRT devices have front and back substrates, phosphors on the inner surface of the front substrates, and electron emitters opposite to the phosphors and excite the phosphors), the method comprising: subjecting a metal substrate to electrolytic oxidation, thereby forming an oxide substrate having a number of small through holes, each of which opens to both surfaces of the metal substrate (see Fig. 5, items 12 and 17; column 5, lines 30-33, lines 52-68); column 6, lines 15-26); burying an electron-emitting material in the through holes of the oxide substrate (see Fig. 4, item 20; column 5, lines 52-53); forming a first electrode on one surface of the oxide substrate, the first electrode contacting the electron-emitting material (see Fig. 4, item 21; column 6, lines 3-7); and forming a second electrode on another surface of the oxide substrate (see Fig. 4, item 23; column 6, lines 3-7), the second electrode insulated from the electron-emitting material (see Fig. 4, item 11; column 5, lines 22-28). Yoshida et al. fail to specifically disclose that the flat panel CRT includes a front and second substrate arranged opposite each other; phosphor layers provided on an inner surface of the first substrate, and an electron source device provided between the first and second substrates, configured tot excite the phosphor layers.

Jin et al. disclose a flat display apparatus including a front and second substrate arranged opposite each other (see Fig. 9, items 140 and 146; column 8, lines 29-44); phosphor layers provided on an inner surface of the first substrate (see Fig. 9, item 144; column 8, lines 29-44), and an electron source device provided between the first and second substrates (see Fig. 9, item 147; column 8, lines 29-44), configured to excite the phosphor layers (see Fig. 9, items 147 and 146). This configuration provides a display device.

Therefore, it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the method of manufacturing an electron source of Yoshida et al. to specifically include a front and second substrate arranged opposite each other; phosphor layers provided on an inner surface of the first substrate, and an electron source device provided between the first and second substrates, configured tot excite the phosphor layers, as taught by Jin et al., to provide a display device.

13. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yosida et al. (U.S. 5,315,206) in view of Jin et al. (U.S. 5,648,699) and in further view of Terai et al. (U.S. 3,935,349).

14. As to claim 13, Yoshida et al. and Jin et al. et al. disclose the method of manufacturing an electron source device, according to claim 12. Yoshida et al. and Jin et al. fail to disclose that the oxide substrate is coated with a mold release agent before the organic substance is introduced.

Terai et al. disclose a method of coating the surface of aluminum oxide with a mold release agent, in this case silane (see the Abstract). Terai et al. further disclose that coating with silane improves aluminum oxide's adhesive property.

Therefore, it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to modify the method of manufacturing an electron source of Yoshida et al. to include a step of treating the insulating layer with a mold release agent, such as silane, as taught by Terai et al., for the added benefit of improved adhesive properties of aluminum oxide.

Response to Arguments

15. The examiner acknowledges the amendments to claims 9 and 13, and the newly added claim 19.

16. In light of the amendment to claim 9, a new rejection has been given.

Final Rejection

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Prior Art

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Burgess et al. (U.S. 4,801,367) discloses a method for electroetching a metal material via oxidation to produce a desired shape.

Yoshida et al. (U.S. 5,648,699) discloses a method for added an organic substance to a field emitter display.

Contact Information

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony J. Canning whose telephone number is (571)-272-2486. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh D. Patel can be reached on (571)-272-2457. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Anthony Canning

28 December 2005

ASHOK PATEL
PRIMARY EXAMINER